disabling the sense amplifier circuitry from driving the bit lines;

selecting a bit line while the sense amplifier circuitry remains disabled; and

providing a current level to a pad in the integrated circuit chip corresponding to a voltage level appearing on the selected bit line while the sense amplifier circuitry coupled to the selected bit line remains disabled.

22. (Amended) An apparatus, comprising:

a random access memory device, comprising:

a memory array of memory cells organized into rows and columns, including a plurality of word lines and bit lines, each row of memory cells being coupled to a word line and each column of memory cells being coupled to a bit line;

sense amplifier circuitry coupled to the bit lines;

address decode circuitry for receiving an address value and asserting a row line associated therewith; and

test circuitry, coupled to at least one bit line for placing on an external pad during a test mode of operation a current level corresponding to a voltage level appearing on the at least one bit line, the sense amplifier circuitry, including sense amplifier circuitry coupled to the at least one bit line, being disabled during the test mode of operation.

37. (Amended) An apparatus, comprising:

a ferroelectric capacitor; and

means for placing on an external pad of the apparatus during a test mode of operation a current level corresponding to a voltage level appearing across the ferroelectric capacitor, comprising a first transistor having a control terminal coupled to a plate of the ferroelectric capacitor, a first conduction terminal coupled to the external pad and a second conduction terminal connected to a voltage reference, and a second transistor having a first conduction terminal connected to the external pad and a second conduction terminal connected to the first conduction terminal of the first transistor, and a means for selectively activating the second transistor during the test mode of operation.

Please add the following new claims 40-49.

40. (New) The random access memory device of claim 1, wherein the current level placed on the external pad by the test circuitry is proportional to the voltage level appearing on the at least one bit line.

41. (New) The method of claim 16, wherein the current level provided to the pad is proportional to the voltage level appearing on the selected bit line.

42. (New) The apparatus of claim 22, wherein the current level placed on the external pad is proportional to the voltage level appearing on the at least one bit line.

43. (New) The apparatus of claim 37, wherein the current level placed on the external pad by the means for placing is proportional to the voltage level appearing across the ferroelectric capacitor.

Cont

44. (New) The apparatus of claim 37, wherein the plate of the ferroelectric capacitor is coupled to a column line, and the control terminal of the first transistor is connected to the column line.

45. (New) The apparatus of claim 37, further comprising a counter having an output coupled to a control terminal of the second transistor.

46. (New) The apparatus of claim 37, further comprising a sense amplifier coupled to the plate of the ferroelectric capacitor, and wherein the means for placing further comprises a disable circuit for disabling the sense amplifier when the current level is placed on the external pad during the test mode of operation.

47. (New) The apparatus of claim 37, further comprising calibration circuitry comprising a third transistor having a first conduction terminal coupled to a second external pad, a second conduction terminal and a control terminal coupled to a third external pad, and a fourth transistor having a first conduction terminal connected to the second conduction terminal of the third transistor, a second conduction terminal connected to the voltage reference and a control terminal coupled to a voltage level to activate the fourth transistor.

48. (New) The apparatus of claim 47, wherein the third and fourth transistors substantially match the first and second transistors, respectively.

49. (New) The apparatus of claim 47, wherein the third and fourth transistors have substantially the same operating characteristics as the first and second transistors, respectively.

REMARKS

Upon entry of the present Amendment, the claims in the application are claims 1-37 and 40-49. Claims 40-49 are new.